SYNOPSYS®
Silicon to Software™

The Evolution of High-Speed PHY IP for Compute & Networking SoCs

D&R IP SoC Days Silicon Valley

Manmeet Walia,
Sr. Product Marketing Manager

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AGENDA

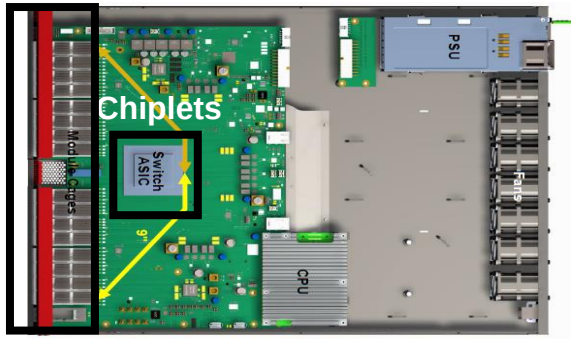
1. Use Cases for Long Reach & Die-to-Die Connectivity
2. Key Care Abouts
3. Differentiated IP Solutions

Long Reach Connectivity Use Cases

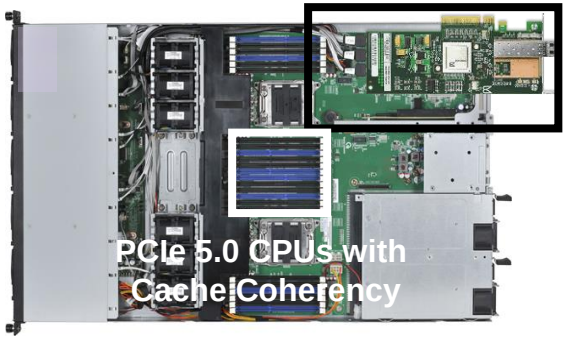
From 100GE to 400GE with Machine-Machine Traffic Growth & Leaf-Spine Architectures

Line Card
8G→16G/25G/32G & USR

Pluggable to Mid-Board Optics



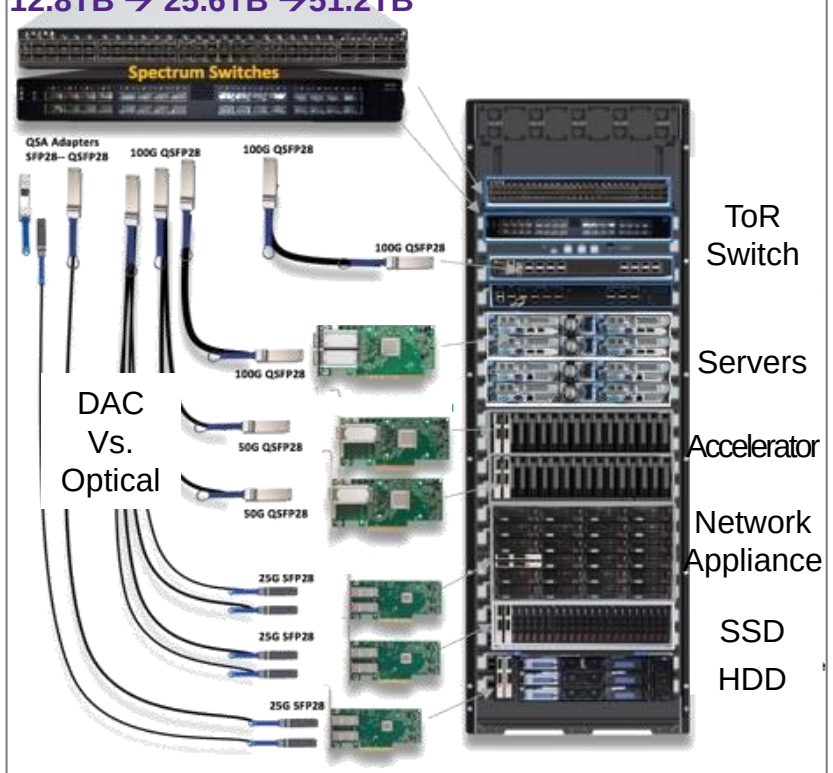
Smart NICs



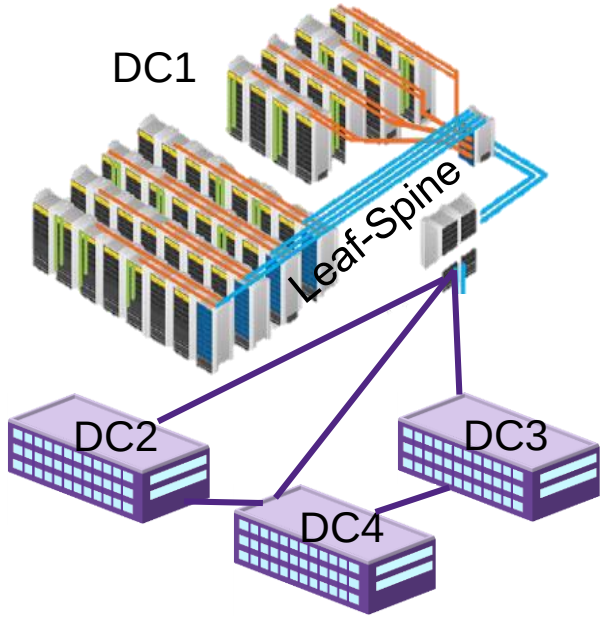
Intra-Rack (ToR)
25/50G → 50/100G

ToR Switch → MoR

12.8TB → 25.6TB →51.2TB



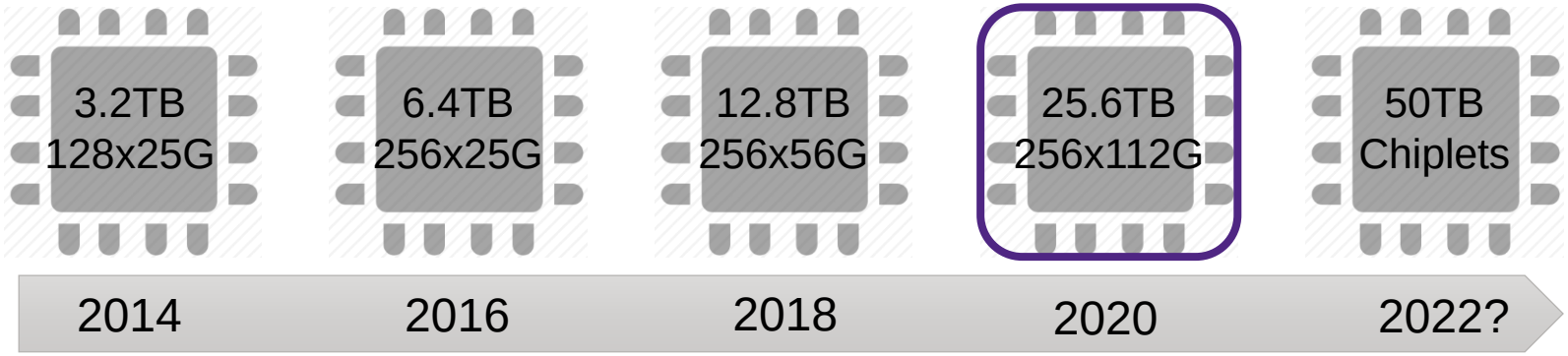
Inter-Rack, Co-Lo & Regional
50/100G → 200/400G

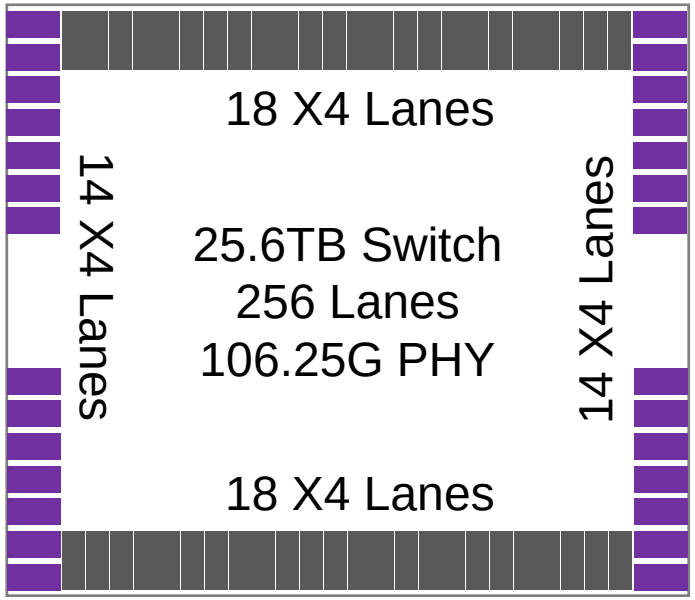


Intra-Rack: 25/50G → 50/100G
Inter-Rack: 25/50G → 50/100/200G
Co-Location: 50/100G → 200/400G
Regional: 100G → 400G

Next Gen. PAM-4 PHYs for Long Reach

Evolution of Top of Rack Switch in Hyperscale Data Centers





Key Careabouts

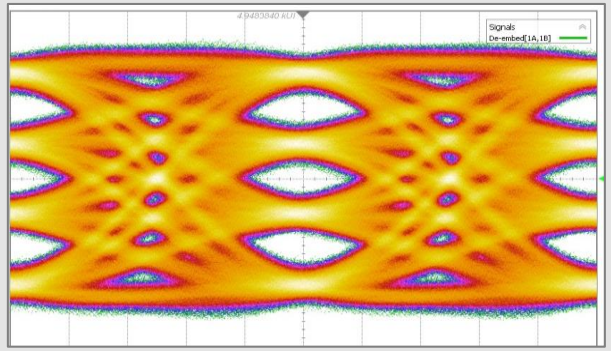
- Area & beach-front
- NW & EW macros
- Power vs. performance
- Robust PVT operation
- Crosstalk performance
- True LR performance
- Overall integration

DesignWare 112G/56G PHYs

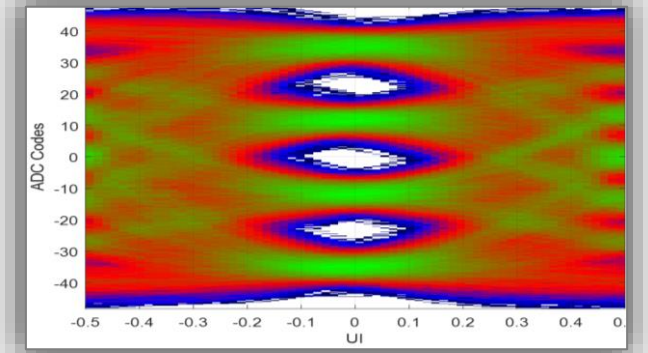
High-Performance Long Reach Connectivity

- Architected for next gen. 400G - 800G data centers, enabling top-of-rack switch connectivity with 5M DAC cables & backplanes
- Comprehensive PAM-4 multi-test chip strategy
  - 7 test chips in advanced FinFET Technologies
  - Customers with silicon in high volume data center & telecom applications
- Exceeds critical J-TOL & I-TOL specs by wide margin with patent pending low latency M-M CDR architecture for a true long reach performance
- Designed for dense networking & HPC SOCs with area efficient 4-lane square macro & unique layout to maximize bandwidth per die-edge through stacking & placement on all 4 edges of the die
- Support for broad range of protocols (Ethernet, OIF, CPRI, JESD, InfiniBand) with independent per lane PLL for data rate flexibility
- Easy thermal budgeting with power scaling techniques, delivering up to 20% power reduction in low loss channels
- Build for harsh data center & telecom environments with robust performance over VT corners with μP based Raw-PCS & performance enhancing algos

106.25Gbps PAM4 TX Eye

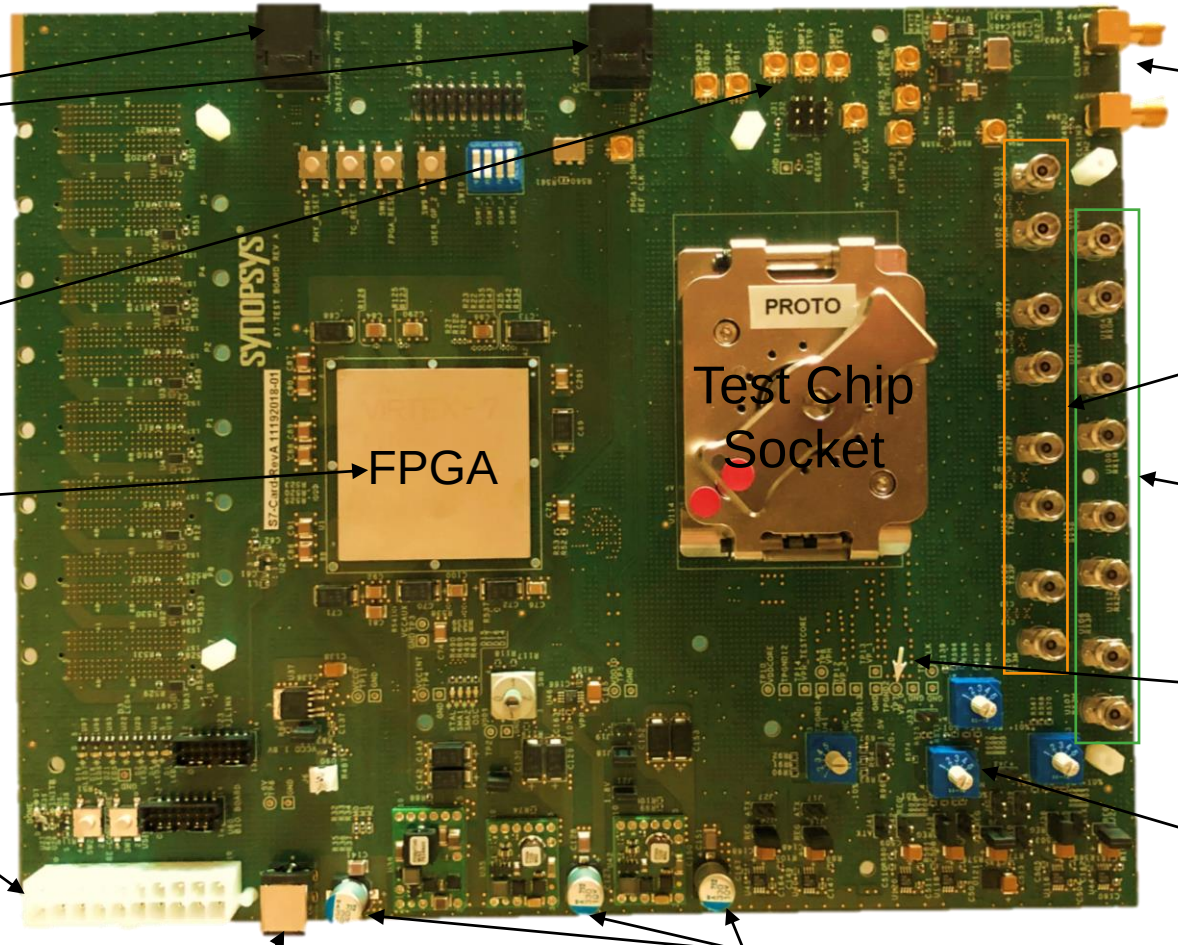


Loopback over 40dB Channel



Synopsys' 112G Ethernet Evaluation Card

Enables Comprehensive Electrical Testing Including Temp Cycling in Customer Chassis



JTAG

Internal Probe

Xilinx Vertex

Direct Power Supply w/o Regulators

Power Supply

Supply Regulators

Reference Clock

High Speed TX 4 Lanes

High Speed RX 4 Lanes

Status LEDs

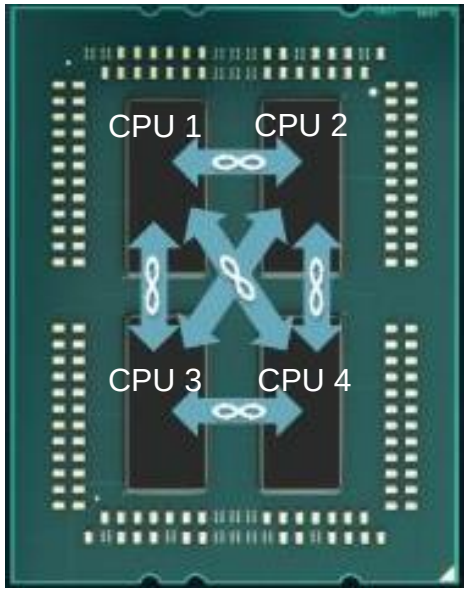
Power Supply Variation Knobs

Two Converging Trends for D2D Connectivity

DesignWare Die-to-Die IP Addresses Key Careabouts For Both Markets

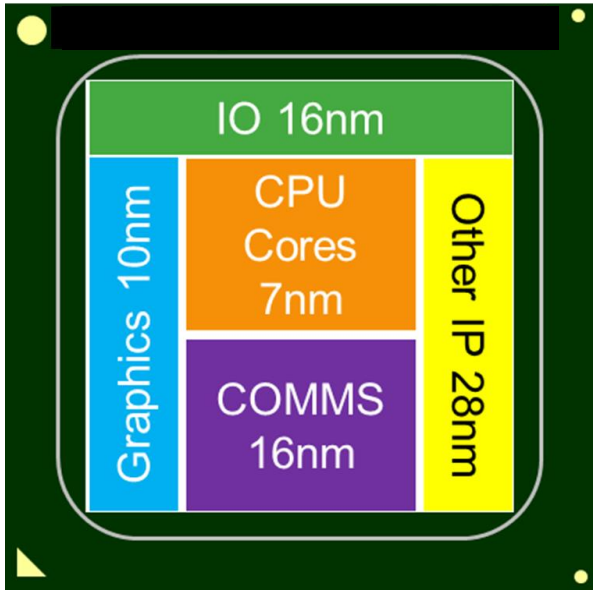
Die Disaggregation (Homogenous Dies)

- Split massive SoCs approaching reticle size
- Improve yield & die cost
- Increase scalability
- Extend Moore's law



Package Integration (Heterogenous Dies)

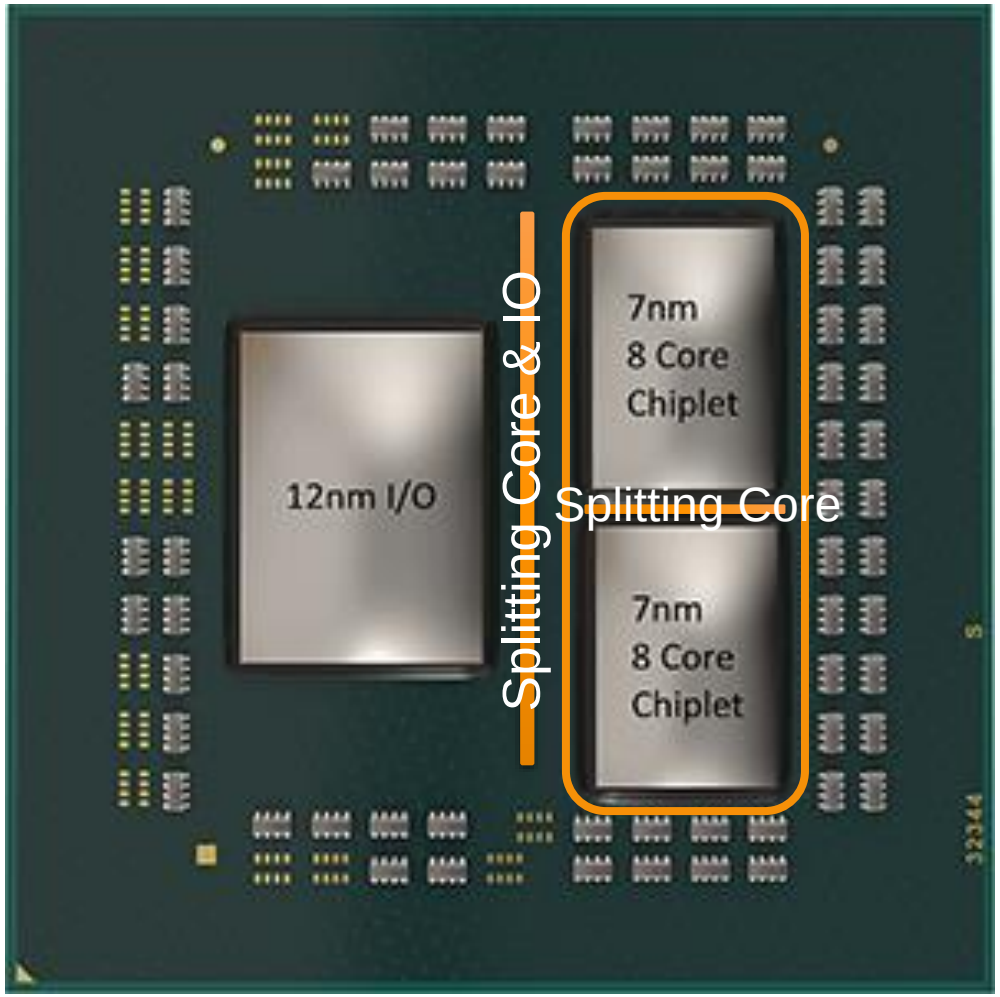
- Bring different functions into same package
- Lower power, smaller form factor
- More flexibility, multiple SKUs etc.
- Reuse, lower risk, lower cost & improve TTM



Server Chip Set

Die Disaggregation; Splitting Dies at Core vs. IO Have Different Careabouts

- **Splitting IO**
  - High bandwidth
  - Longer reach
  - BER is less important as it is managed with end to end protection

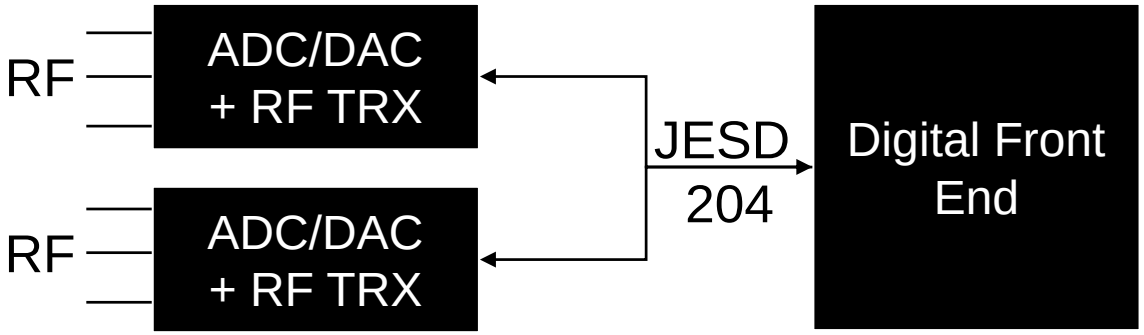


- **Splitting Cores**
  - 2 CPU dies acting like a single CPU
  - Low latency
  - Low BER
  - No FEC

5G Wireless Infrastructure

Package Integration; JESD 204 Interface Replaced by USR SerDes

Multi-Chip Solution with JESD 204 Interface

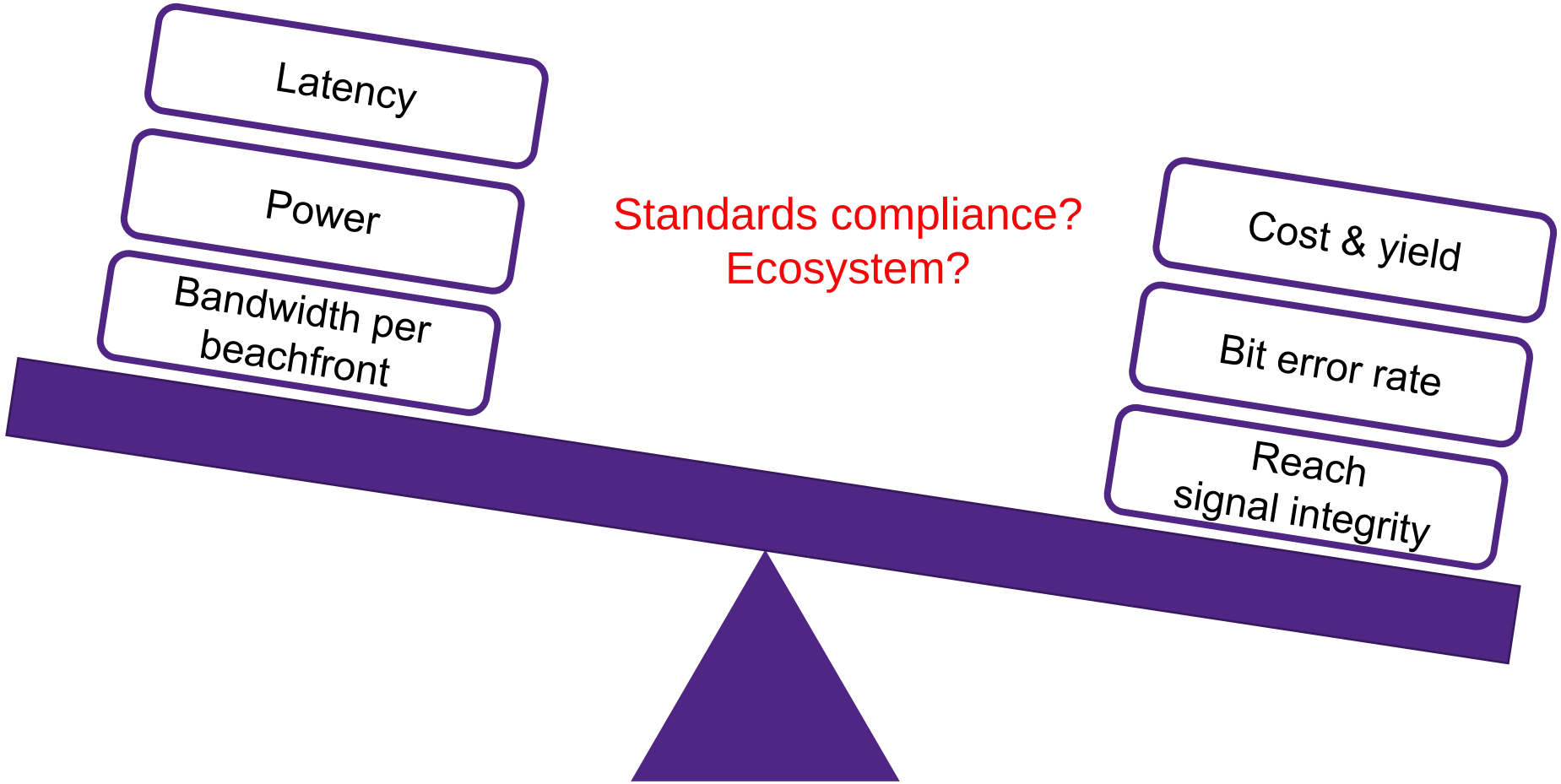


Dies in Single Package with USR Interface

- Package integration use case
  - Heterogeneous dies
  - Digital front end in 7nm
  - ADC/DAC + RF TRX in 12nm or 16nm
- Key Objectives
  - Reduce power
  - Smaller form factor
  - Process node optimization per function
  - Reduce Latency
  - Standardization @ JEDEC (TAT 2022)
  - Re-use, lower risk and TTM

Critical Metrics for Die-to-Die Connectivity

One Size Does Not Fit All…



Die-to-Die PHY Options

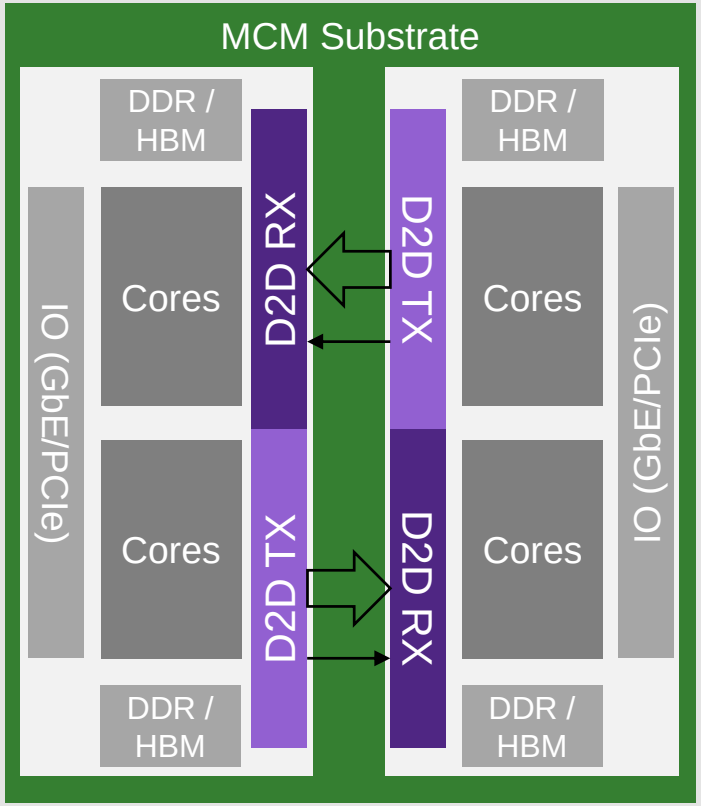
Multiple Solutions have Emerged that Allow Trade-Off of Critical Metrics

	Serial Interface (PAM-4)	Serial Interface (NRZ)	Parallel Interface
Specifications	OIF CEI 112G URS/XSR	OIF CEI 56G URS/XSR	OpenHBI, AIB, BoW
Data rate per Lane	56Gbps to 112Gbps	2.5Gbps to 56Gbps	2 to 4Gbps → 6Gbps
Bandwidth/beachfront	High ✓	Low	High ✓
Power	1.0 pJ/bit	1.5 pJ/bit	0.5 to 1.0 pJ/bit ✓
Latency	Higher	Low ✓	Low ✓
Bit error rate (BER)	Requires FEC in PAM-4	Reliable link ✓	Reliable link ✓
Packaging technology	Standard (substrate) ✓	Standard (substrate) ✓	Advanced (interposers)
Overall cost	Low ✓	Low ✓	High

DesignWare Die-to-Die Solutions

112G USR/XSR & HBI/AIB PHYs

- SerDes & Parallel-based Die-to-Die PHY IPs support most packaging technologies
  - 112G USR/XSR SerDes compliant with OIF CEI-56G/112G standards
  - Parallel PHY compliant with AIB and HBI standards
- Area optimized macros enable maximum placement flexibility and high bandwidth/beachfront
- Protocol agnostic Raw-PCS implements all calibration, adaptation and other advanced algorithms for robust operation over VT
- Built-in loopbacks, testability and diagnostics features provide increased testability & coverage for known good dies
- Low latency data path architectures provide ideal solution for die disaggregation in MCMs for Server & AI applications
- SI-PI and Integration services to assist customer use of IP

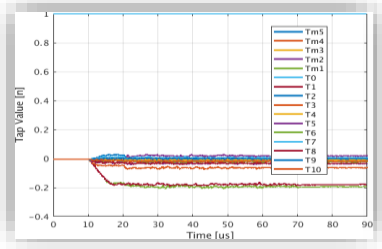


Synopsys Differentiation

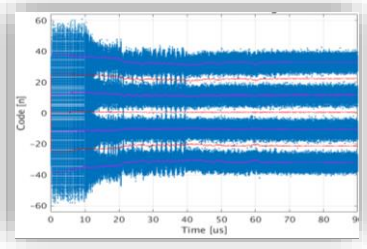
Comprehensive Integration & Support

Integration

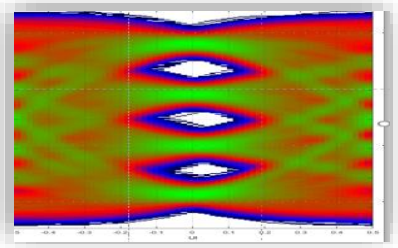
- Flexible metal stack (11 Min, Top 2 thick)
- Flexible bump pitch with support for Cu-Pillar & micro-bumps
- Optimized placement on 4 edges of die
- Reference clock forwarding for integrating multiple instances
- Extensive test features include ACJTAG, SCAN, IDDQ/Burn-in, RX eye monitor



FFE Taps



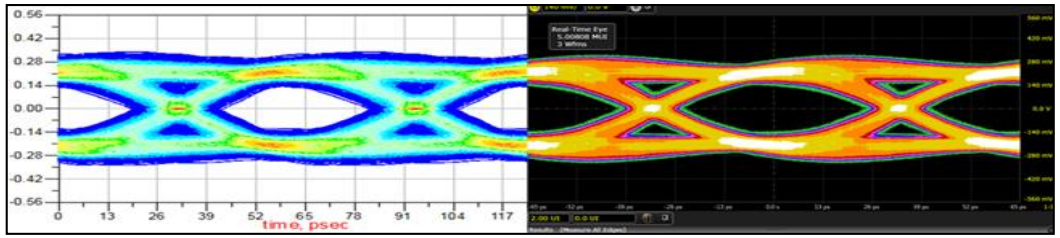
Scatter Plot



RX Eye

Support

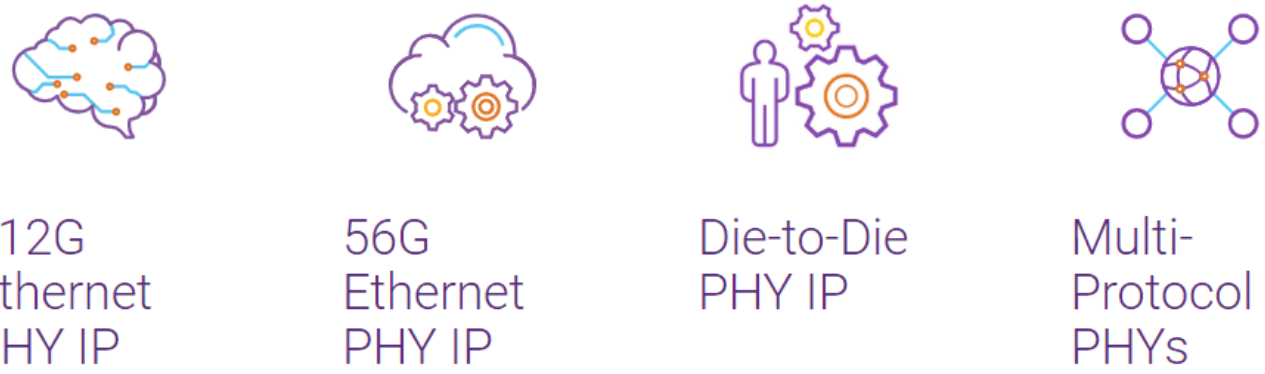
- Tightly integrated deliverables; optional early enablement with front end kits
- PCB & Package substrate design guidelines
- Silicon Correlated IBIS-AMI Models for Accurate Signal Integrity Analysis
- Hardware support include prototyping kits
- Support & Integration Reviews



Simulated (IBIS AMI)

Measured

Synopsys: The Most Trusted High-Speed PHY IP Provider



- IP solutions for 800G SoCs: DDR5/4, HBM, PCI Express 5.0, 112G Ethernet, Die-to-Die, CXL
- Adopted by leading data center companies
- Available in advanced process technologies from 16-nm to 7-nm FinFET, with 5-nm in design
- 112G Ethernet PHY for long reach connectivity over backplane, copper cables, & optical links & successfully tested with 40dB+ Backplanes & 5 Meter Copper Cables
- 112G USR/XSR PHY for die-to-die connectivity over organic substrate & InFO
- HBI/AIB PHY for die-to-die connectivity over interposers & InFO
- Comprehensive support for easy IP integration into SoCs

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Thank You