chipus

Low Power Applications at the "Edge" in the Infamous IoT Space

By Elias Lozano
SVP of WW Sales and BD

April 9th, 2020

Outline

1. About Chipus
2. IoT Edge Devices: Challenges & Opportunities
3. Chipus methodology
4. Typical IoT chip at the “edge”
5. Technical case study: Battery charger
6. Success cases
7. Conclusion

Chipus mission

Chipus Mission

"Develop chips that enable **innovative** and **power efficient** products"

Chipus has been delivering **tailormade ASICs**, ultra low power analog IP, efficient power management circuits and for **more than 10 years**.

Company

Chipus facts

- Founded in 2009
- Successfully delivered projects to customers in:
  - North America
  - Europe
  - Asia
- ISO 9001 certified since 2017

- Global presence
  - Office in Santa Clara
  - Business development in the USA and Europe
  - Headquarters and Design Center in Brazil

[Link to Design & Reuse about ISO 9001 certification]

BUREAU VERITAS
Certification

CHIPUS MICROELETRÔNICA S.A.

Rua Emílio Blum, 131, 10° Andar, Torre A, Centro, 88020-010 - **Florianópolis/SC**
Brazil

Bureau Veritas Certification certify that the Management System of the above organization has been audited and found to be in accordance with the requirements of the management system standards detailed below

Standards

ISO 9001:2015

Scope of certification

INTEGRATED CIRCUITS DESIGN

Certification cycle start date: **20 November 2017**

Subject to the continued satisfactory operation of the organization's Management System, this certificate expires on: **19 November 2020**

Last Expiration Date: **NA**

Last Certification Audit Date: **14 November 2017**

Original certification date: **20 November 2017**

Certificate No. **BR027127** Version: **1** Revision date: **21-11-2017**

Luiza Negrão, Technical Manager

Local office: *Av. Alfredo Egídio de Souza Aranha, 100, Torre C, 4°Andar Vila Cruzeiro, 04726-170 - São Paulo/SP - Brazil*

CCS 0006

Further clarifications regarding the scope of this certificate and the applicability of the management system requirements may be obtained by consulting the organization.
To check this certificate validity please call +55113955 9000.

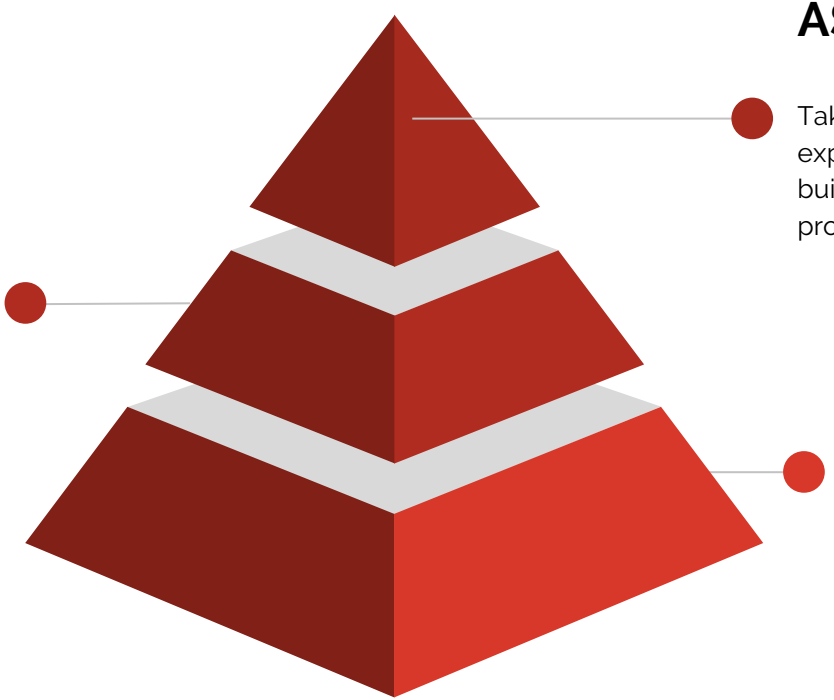
BUREAU VERITAS

Chipus Services

Chipus is a one-stop shop for semiconductor design

Design services

Develop **custom circuits** and **retarget Chipus' IPs** using **best-in-class support** in order to help you develop a successful product



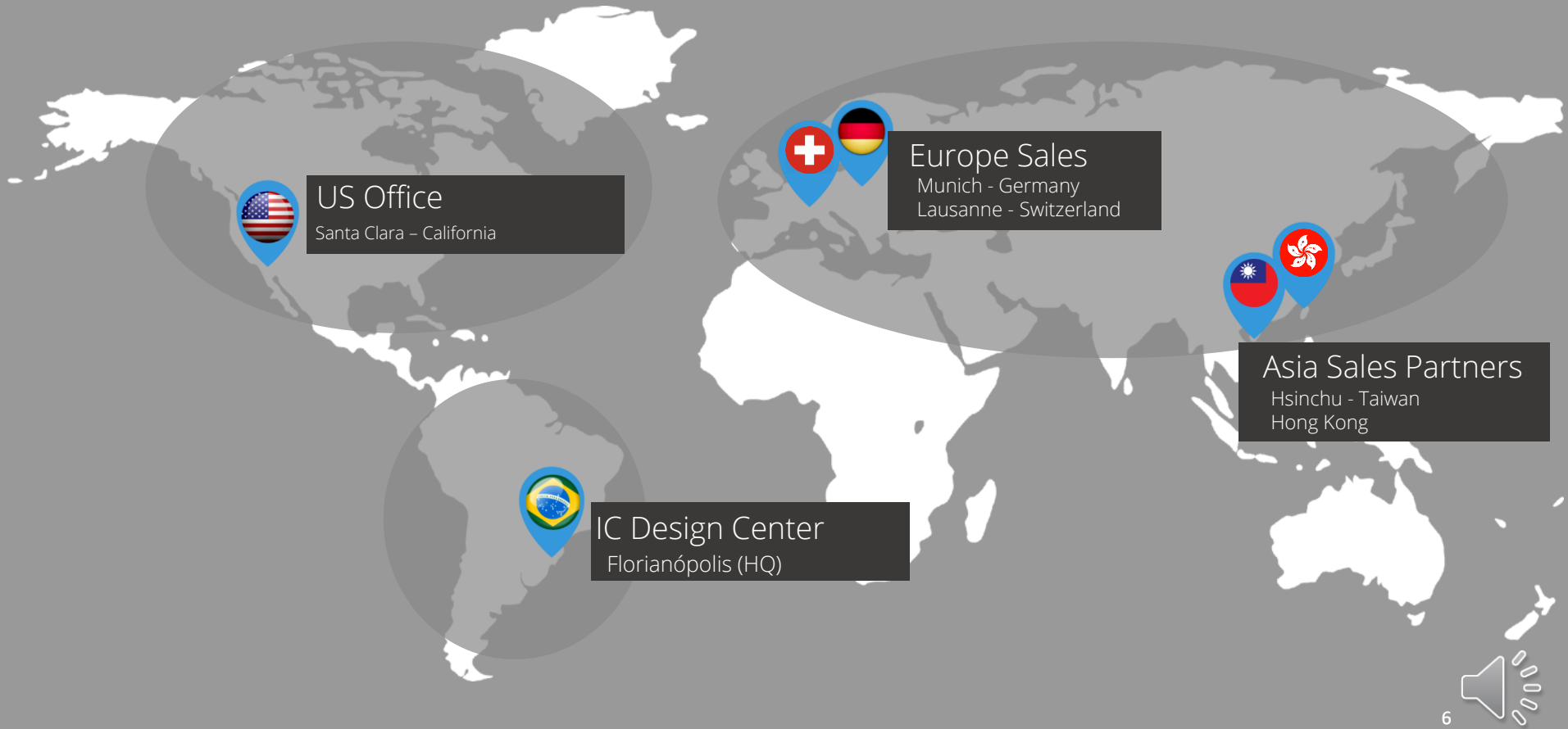
ASIC

Taking advantage of the in house experience, Chipus is enabled to build **turn-key ASIC solutions** with proven success cases

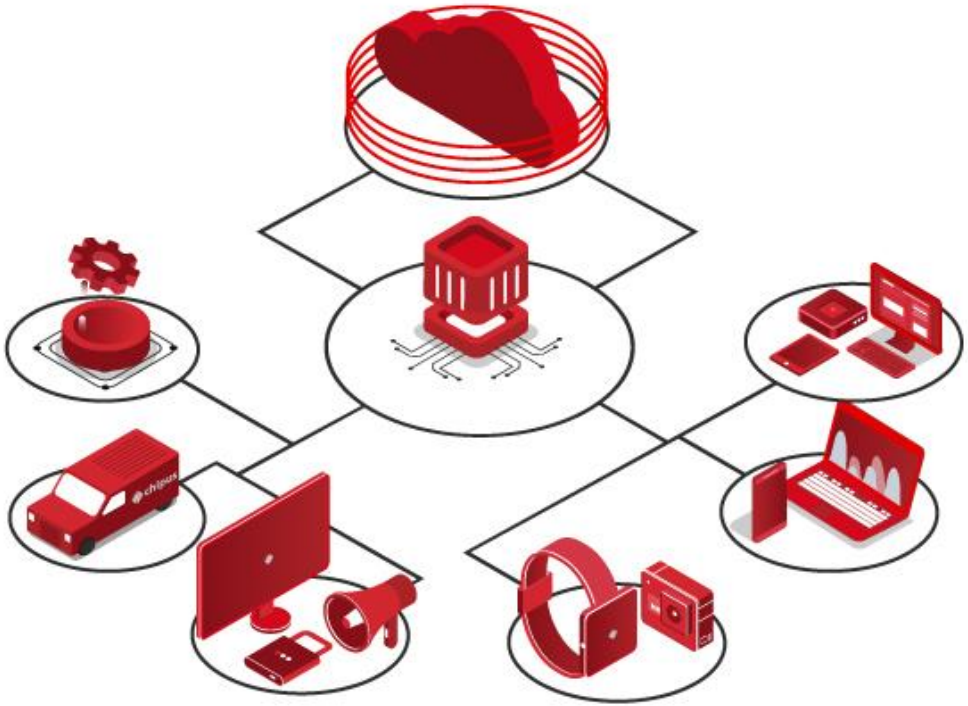
Analog IP

Based on a wide **proven IP** portfolio built over **10 years** in the market, Chipus can provide you the **ultra low power**, **analog** and **mixed signal** IP block you are looking for.

Company


US Office
Santa Clara – California
Europe Sales
Munich - Germany
Lausanne - Switzerland
Asia Sales Partners
Hsinchu - Taiwan
Hong Kong
IC Design Center
Florianópolis (HQ)

IoT Edge Devices: Challenges & Opportunities



Famous IoT architecture

- Cloud services demand big data centers
- Gateways and aggregators will have a standard specifications
- Things are closer to people

IoT Edge devices are close to people

- **Huge** number of “things”
- Diverse applications
- Diverse requirements

IoT Edge Devices: Market Segments

Precision agriculture

- Long time in the field
- Low requirements for bandwidth
- Low requirements on uC
- No access to maintenance
- Custom sensor AFE

Modern wearable device

- Frequently charged
- High requirements for bandwidth
- High requirements on uP
- Quick access to maintenance
- Custom sensor AFE

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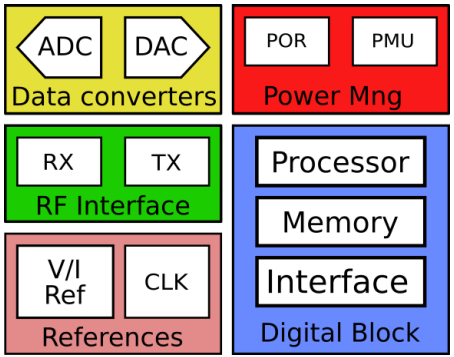
Both solutions demand custom chips

IoT Edge Devices: System Architectures



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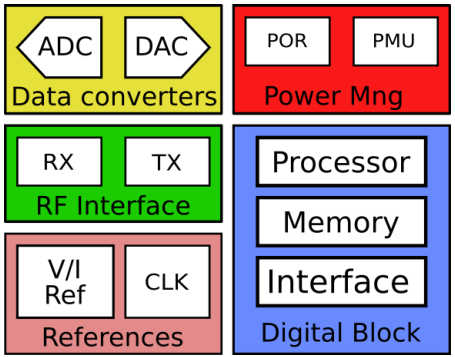

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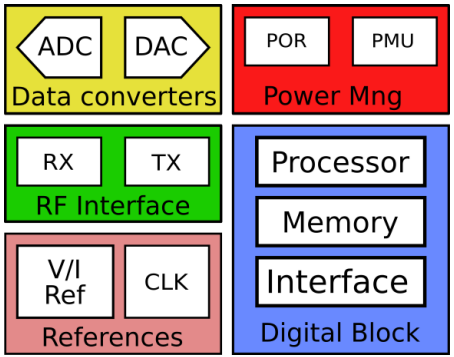
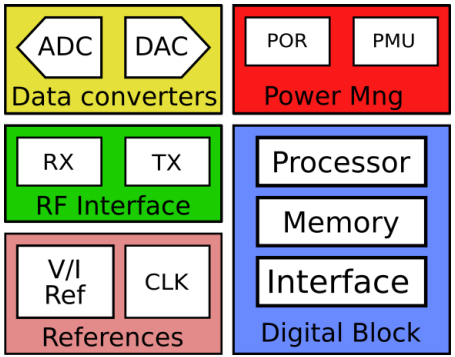


Are they really the same?



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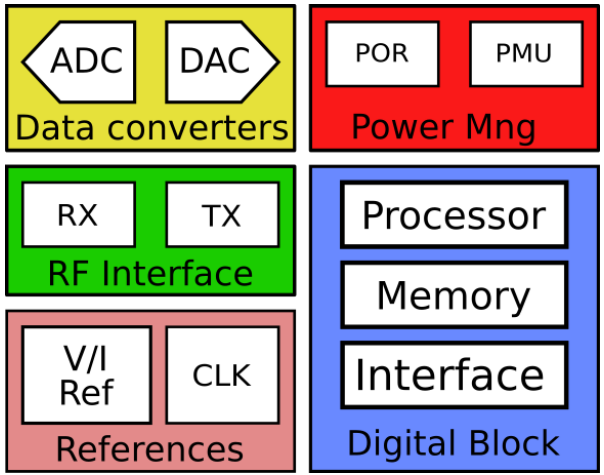


Understanding trade-offs and **building specifications** is part of Chipus' know-how

ADCs
- Sigma-delta
- SAR
- …

DACs
- Sigma-delta
- Current steering
- …

RF Interfaces
- Bluetooth
- LoRa
- WiFi
- …

Power management
- LDOs
- DC/DCs
- …

Processors
- Processor type
- Data bus
- DMIPS

Memories
- NVM
- SRAM
- OTP
- …

Interfaces
- I2C
- MIPI
- SPI
- …

Chipus ASIC mixed-signal Design Methodology

Chipus counts on structured mixed-signal methodology to achieve first-working silicon

Based on checklists, design reviews and supported by ISO procedures
Our IP porting methodology takes advantage of validated testbenches of proven IPs

Specification Capture Phase	Design Implementation Phase	Physical Implementation Phase	Sign-off Phase	Product Support Phase
Chipus + Customer	**Chipus + Customer (reviews)**	**Chipus + Customer (reviews)**	**Chipus + Customer**	**Chipus + Customer**
Chipus will work with customer to mature a set of specifications that fit the product and its manufacturing while enabling the design team to work efficiently.	Chipus' design team will reuse existing IP to speed up the development of the ASIC. Thorough verification will be made to check every specification in all operating condition. Customer is invited to participate in joint design reviews specifically in ATE for manufacturing	Building on top of the documentation from the design team, physical implementation takes all best practices in account to achieve performance and robustness. Layout reuse is also used to speed up the development.	Deep checks are made in the sign-off phase such as top level DRC, LVS, DFM, functional verification and appropiate requirements for ATE development. The design team also runs final checks on the functionality of the ASIC for tape-out.	Chipus supports the customer in the development of system prototypes , end products and full release-to-production manufacturing

Digital Design Capabilities

Design/Functional Verification

- Modeling
  - SystemVerilog
  - SystemC
  - Python
- RTL design
  - Verilog
  - VHDL
- Testbench
  - Verilog
  - SystemVerilog
- Methodology
  - UVM

Logic Synthesis/ATPG

- Logic synthesis
- Insertion of DFT structures
- ATPG

Structural Verification

- Logic Equivalence Check (LEC)
- Static Timing Analysis (STA)
- Power Analysis (EM/IR)
- Physical Verification (DRC/LVS)

Design Implementation

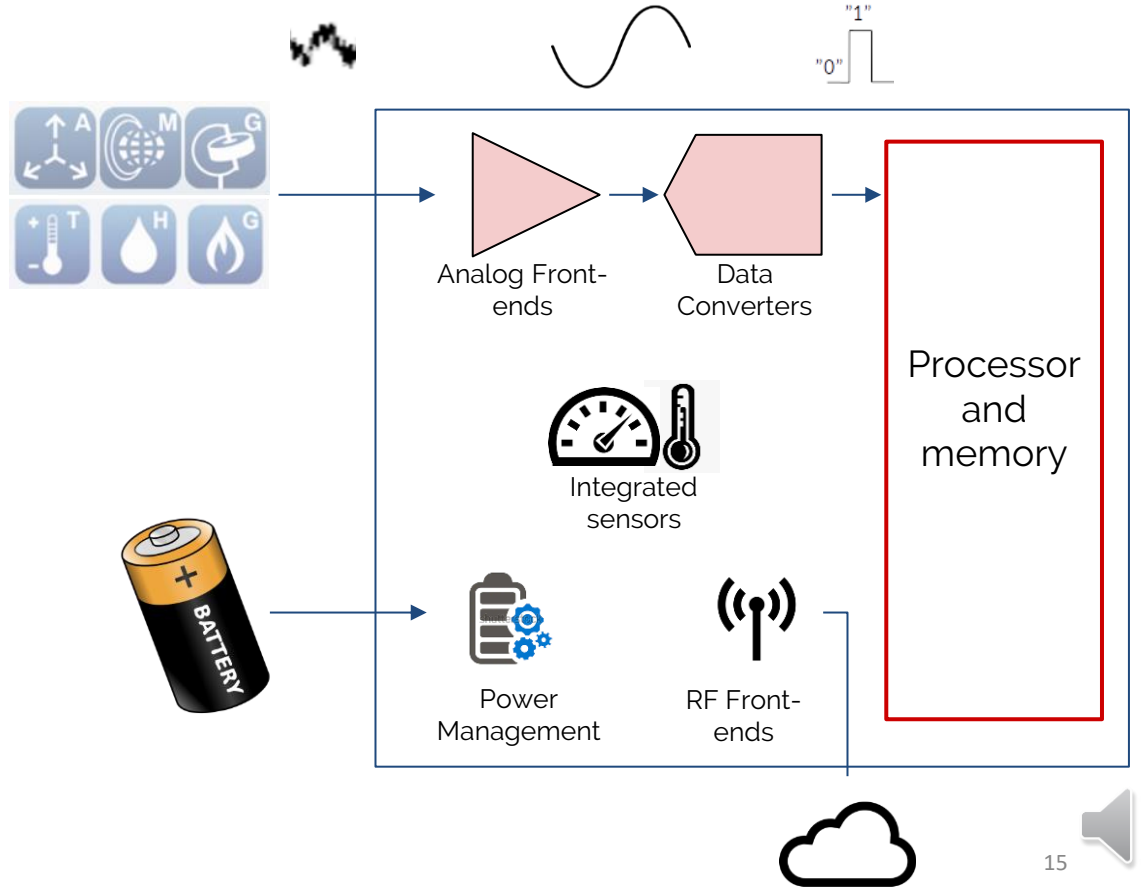
- Floorplan
- Power Plan
- Placement
- CTS
- Routing
- Signal Integrity
- Timing closure

Digital flow implemented with Cadence, Synopsys and Mentor tools

Typical IoT chip at the “edge”

Device at the “edge”

- Acquire from sensors
- Convert data
- Process and store
- Manage power efficiently
- Send data and receive commands



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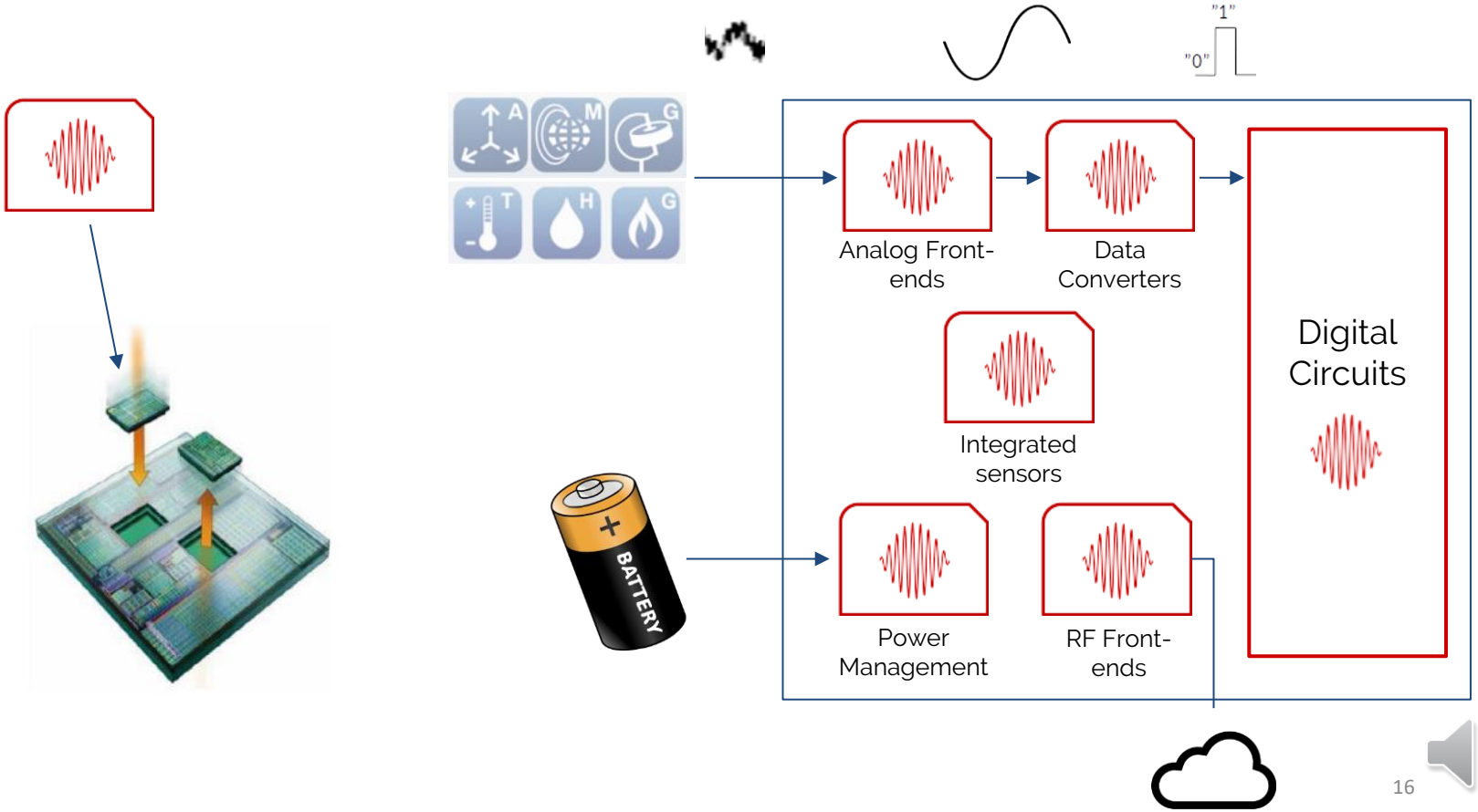

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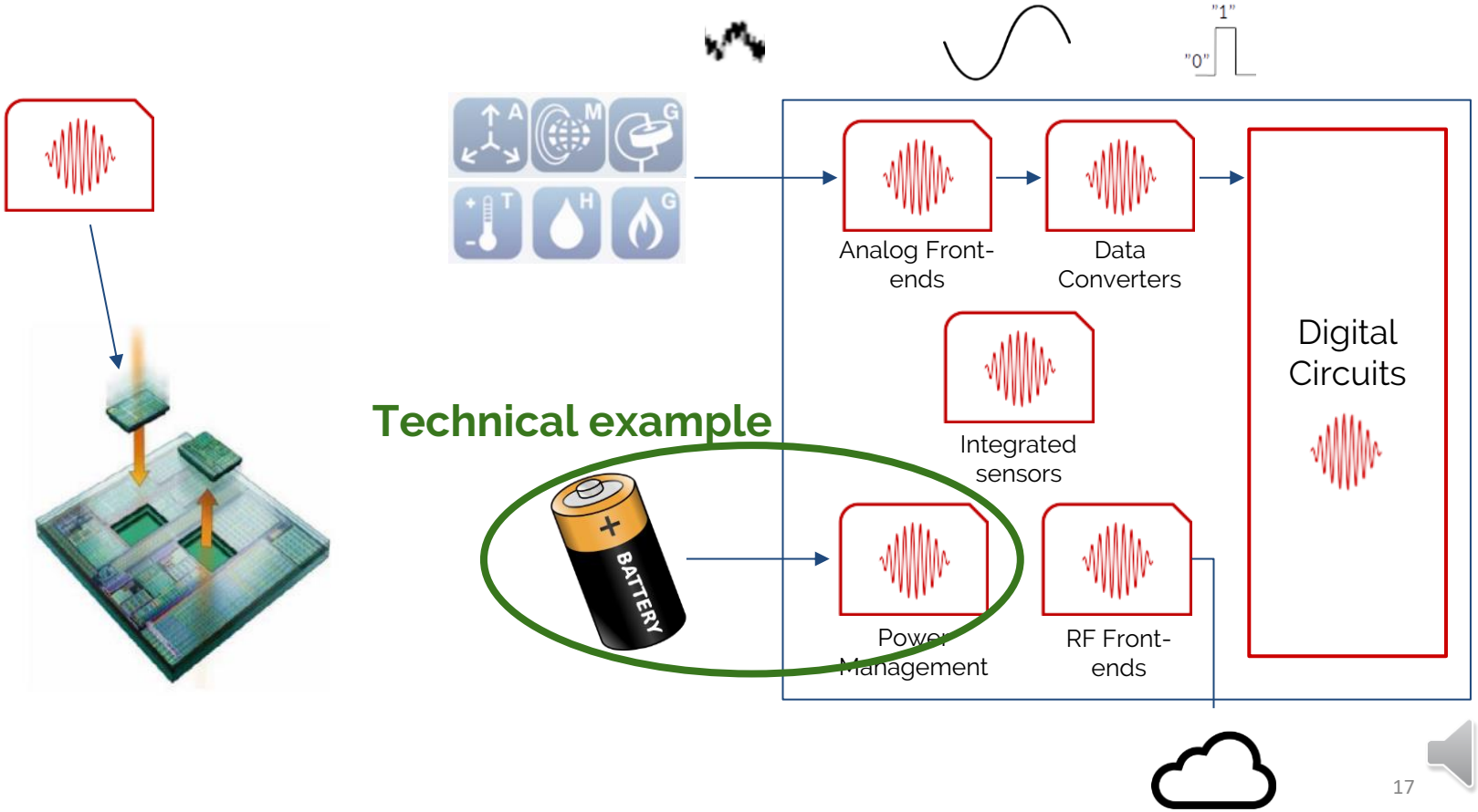
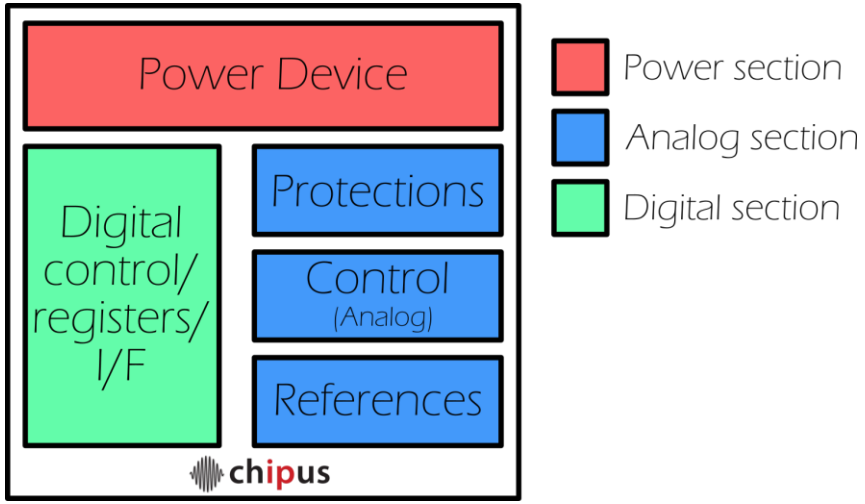


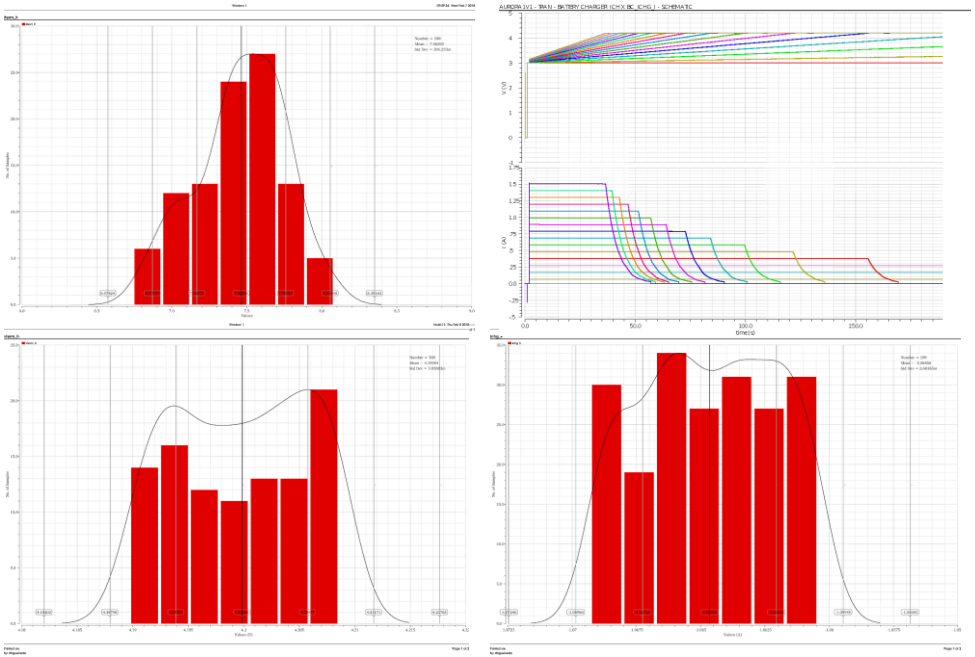
Case Study: Battery Charger



Battery charger is a mixed signal IP that requires care in the design in several levels

- **Analog variations and mismatches**
  - References
  - Buffers
  - Isolation from substrate noise
- **High power sections**
  - Current handling
  - Proper bulk biasing
- **Digital Section**
  - Correct functionality
  - Register mapping
  - Communication interface
- **Integration**
  - Several voltage domains
  - Thermal issues
  - Noise issues

Case Study: Battery Charger



Analog checks include:

- **Several power up conditions**
- **Several operating conditions**
- **Verification of operation modes**
- **Verification of configurable performances**
- **Trimming**

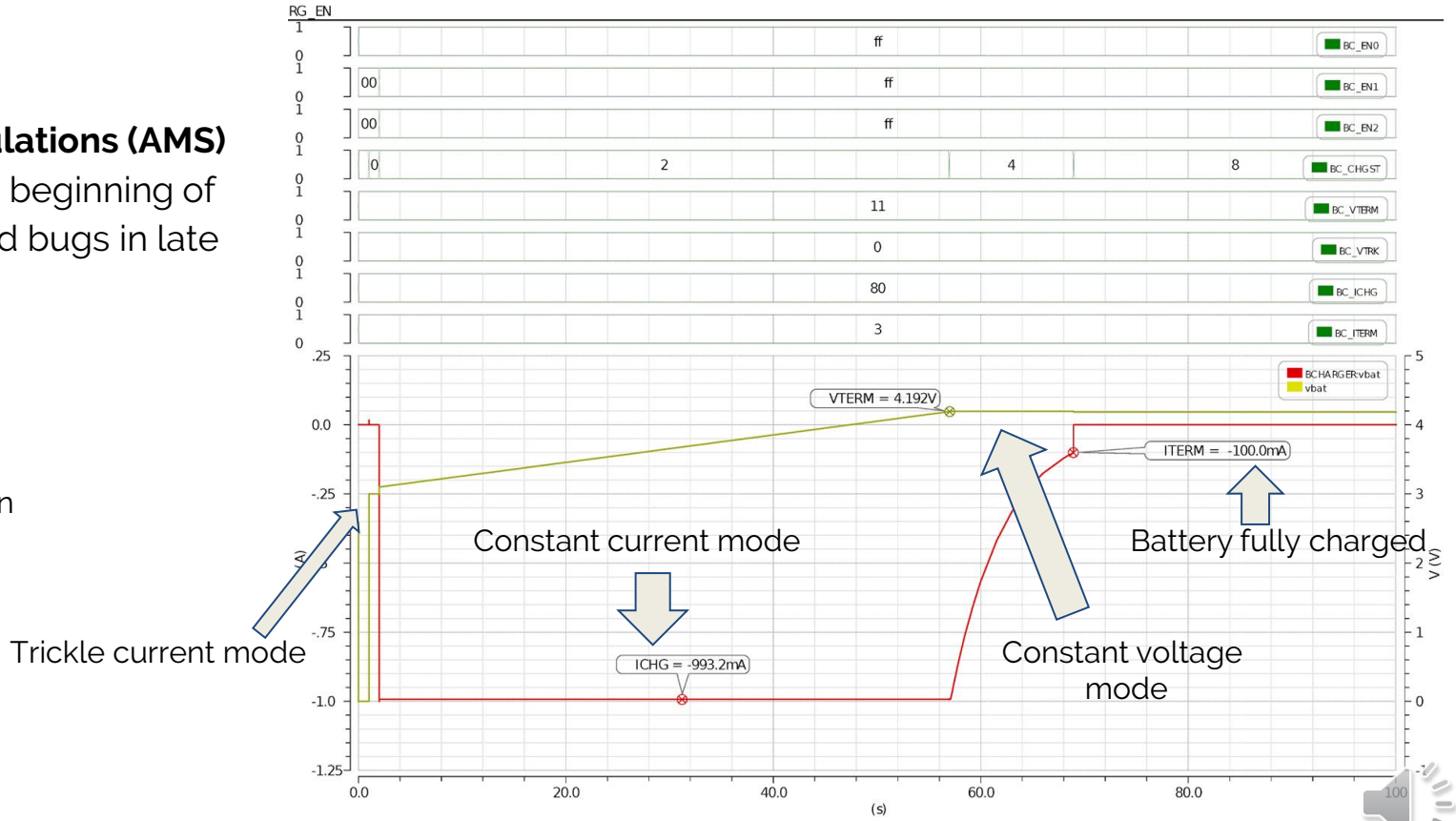
These checks must take into account:

- **Validation across corners**
  - **Process**
  - **Voltage**
  - **Temperature (-40°C to 125°C)**
- **Monte Carlo checks**

Case Study: Battery Charger

Mixed signal simulations (AMS) are used since the beginning of the project to avoid bugs in late phases.

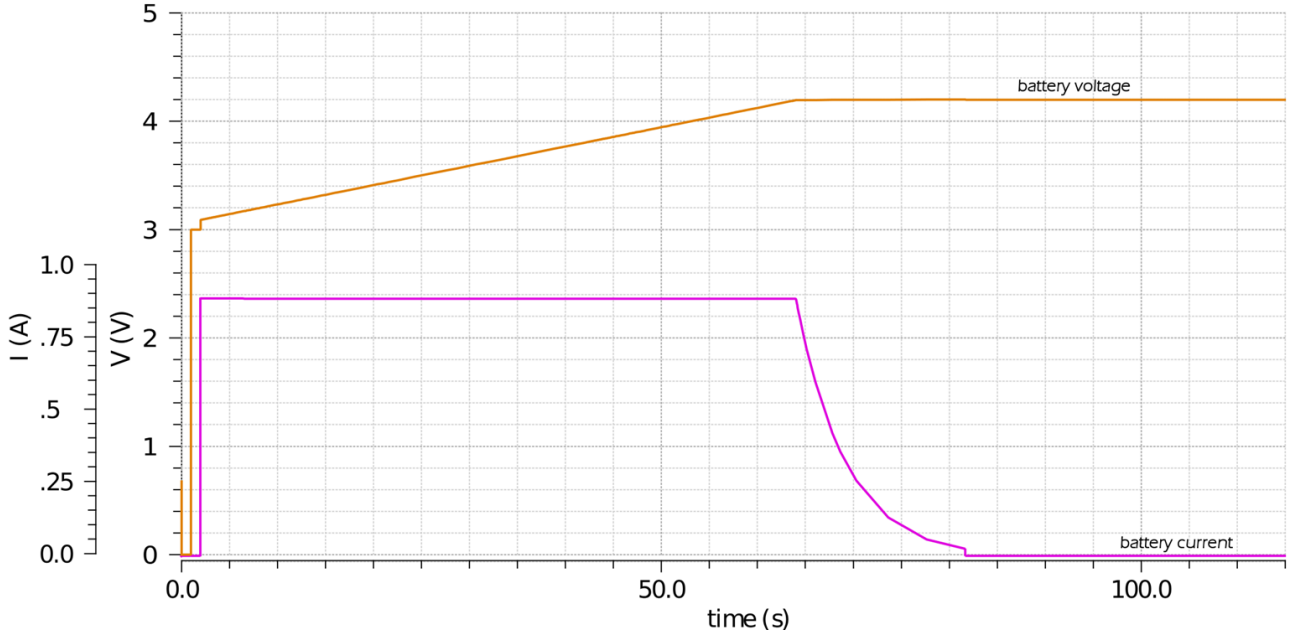
- Flags
- Registers
- Protections
- Trimming
- Communication
- …



Case Study: Battery Charger

In the overall functionality this type of curve is what we are looking for in silicon measurement

Simulation results

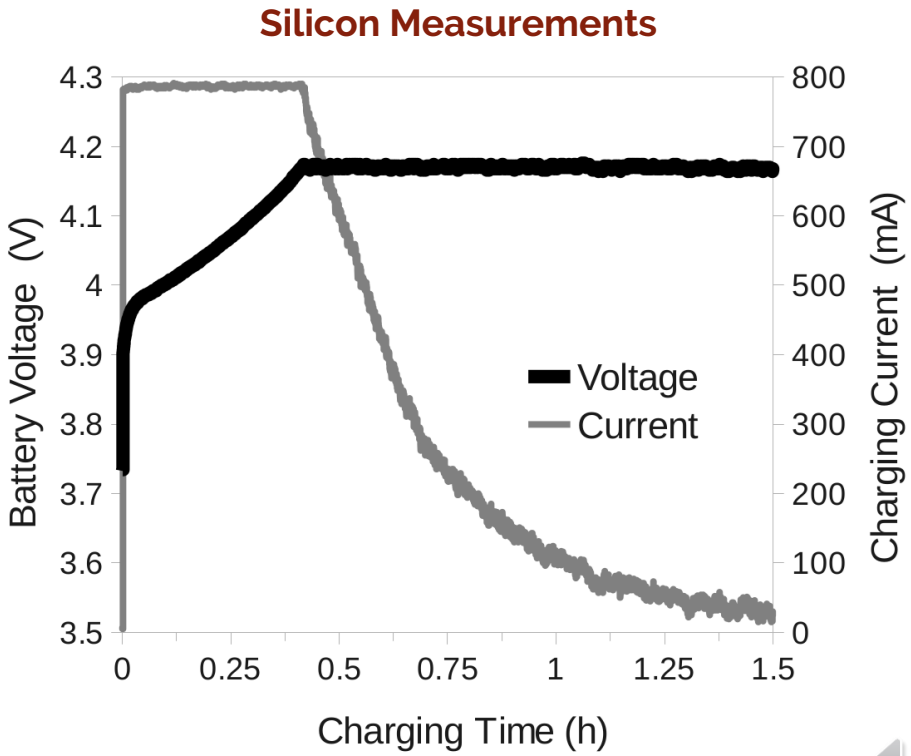


Case Study: Battery Charger

The IPs implement the following charging modes for best battery management:

1. Trickle: IP applies low current until battery voltage is in safe range
1. Fast: full charging current (configurable)
1. Constant voltage: IP keeps constant voltage until battery is completely full

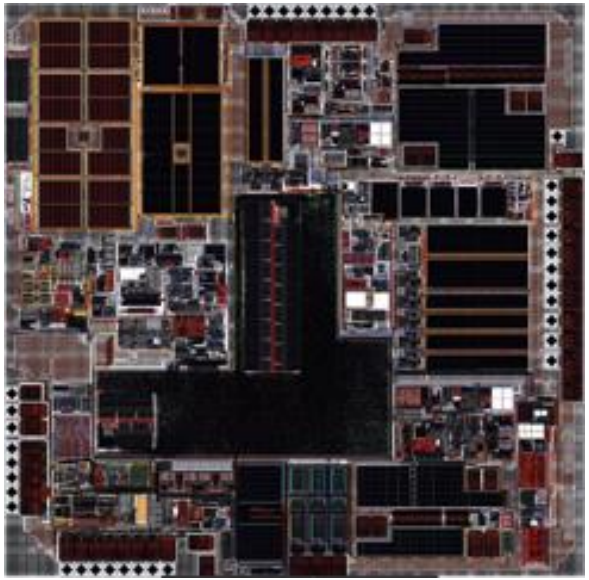
This is obtained after thorough verification in both design and layout phases



Power Management ASIC

Some Information

- 3 DC-DCs (2 bucks and 1 boost) up to 500mA
- Battery Charger up to **1.1 A**
- LED Drivers (4x) up to 300mA
- Load switches up to 100mA
- Ultra-Low-Power LDOs/References/Osc/POR
- USB interface for battery charging
- Ultra-low-power **(350 nA)** in idle mode
- Node: 0.18µm BCD



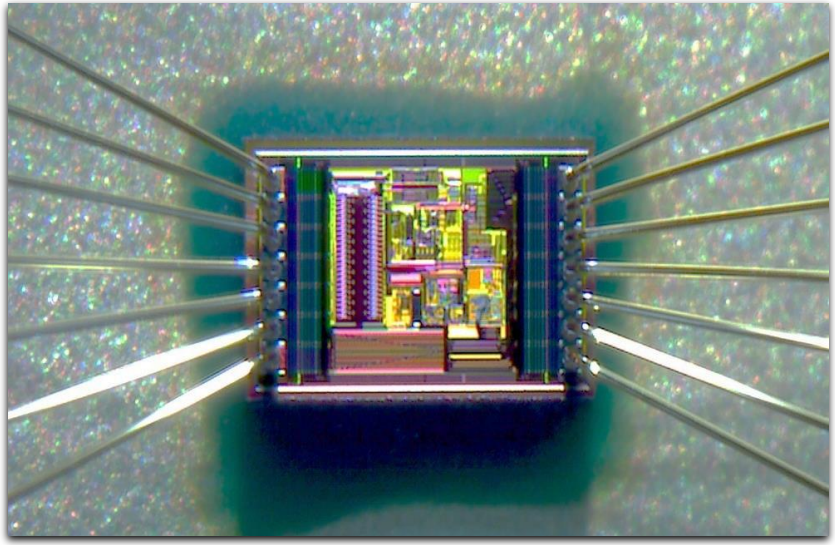
Main Challenges:

1. **Big power transistors (total load up to 1.8A) while having a stand-by mode of only 350nA. Leakage optimization at device level required;**
2. **Cannot use duty-cycle to reduce consumption (Power Management is the only chip that needs to be "on" in the system even in sleep mode).**

Magnetic Sensor ASIC

Some Information

- Integrated Magnetic Sensor
- Integrated Sensor
- Ultra-low power (**250 nA**)
- Specs to Production in 18 months
- Node: 0.13µm CMOS
- Status: **In Production since Q4/2016**



Main Challenges:

1. **Wake up, measure, send data, sleep in the shortest time possible using duty-cycle techniques to optimize consumption**
2. **Innovative sensor technology (custom analog front-end design)**

Chipus analog IP portfolio

Chipus counts on more than 200 silicon-proven mixed-signal IPs to speed up ASIC development

- Power management
  - High voltage
  - High current
  - Low power
  - High efficiency
- Data converters
  - ADCs and DACs
- Integrated sensors
  - Temperature
  - Capacitive touch
  - Magnetic
- Optical
  - Analog Equalizers (<28Ggps)
  - TIAs, PAs
- RF
  - RFID front-ends
  - RF Transceivers

- Processes
  - CMOS
  - BCD
  - SOI
  - SiGe
- Nodes
  - 0.18um
  - 0.13um
  - ...
  - 40nm
  - 22nm
  - 7nm

- Applications
  - Consumer
  - Industrial
  - Automotive
  - Optical communications
  - Medical
  - Wearables

Conclusions

- IoT at the “edge” demands custom chips due to specific requirements
- Interesting opportunity for ASIC companies
- Chipus is ready to provide effective solutions based on:
  - proven expertise over the years
  - extensive analog and digital IP portfolio
  - Porting of proven IPs to reduce time to market
  - Strong Analog and Digital knowledge
- Project methodology transforms specifications into parts
  - Based on ISO procedures
  - Checklists
  - Design reviews with customer
  - Flexibility to adapt to customer
- Our customer’s sucess is also our success as shown in all of our ASIC engagements

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Thank you