

THALES

INVIA
IPs securing ICs

Why should your next secure design be PUF based?

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Design & Re-Use Bay Virtual Event Apr 20

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Introduction to Embedded Security And Cryptography

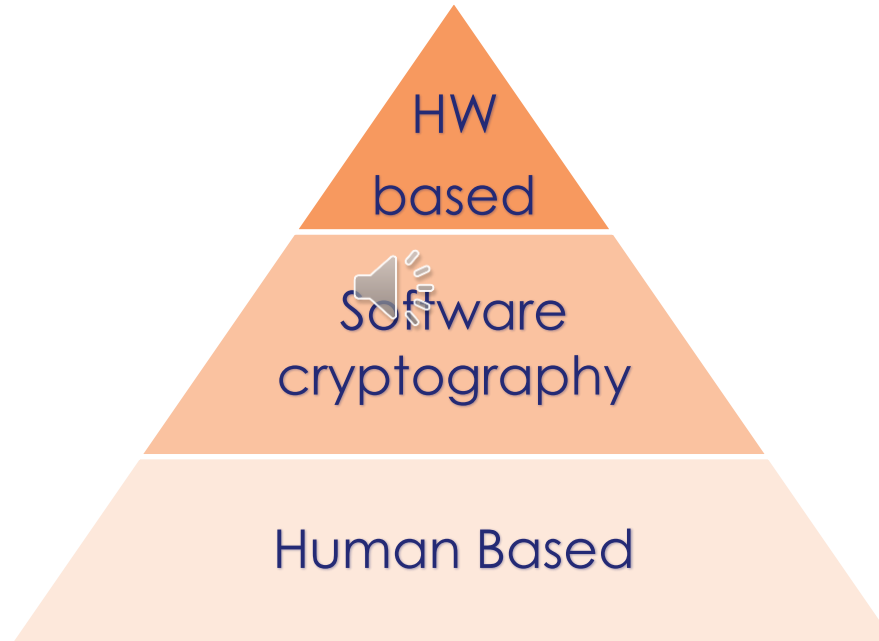
Keys Protection Challenge

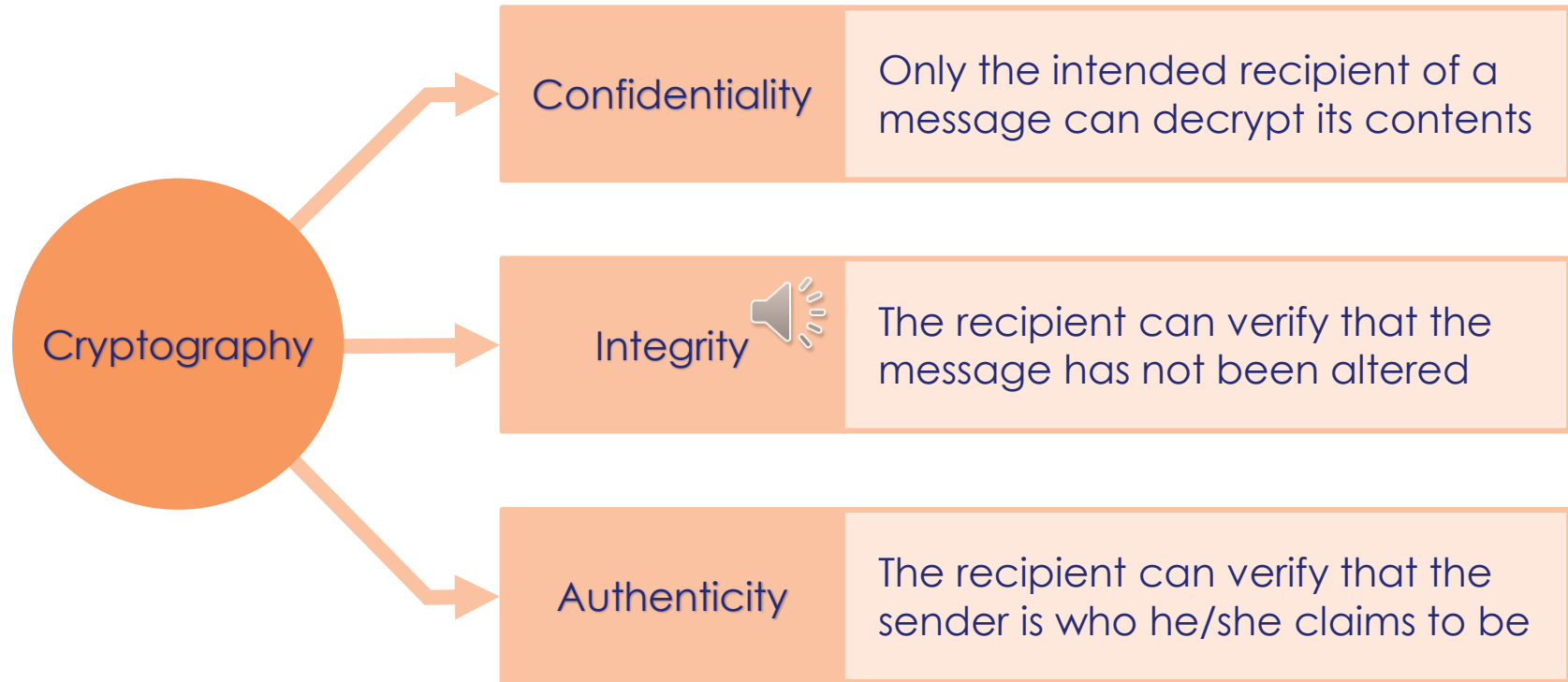


PUF Fundamentals

INVIA's PUF Solution And Its Benefits

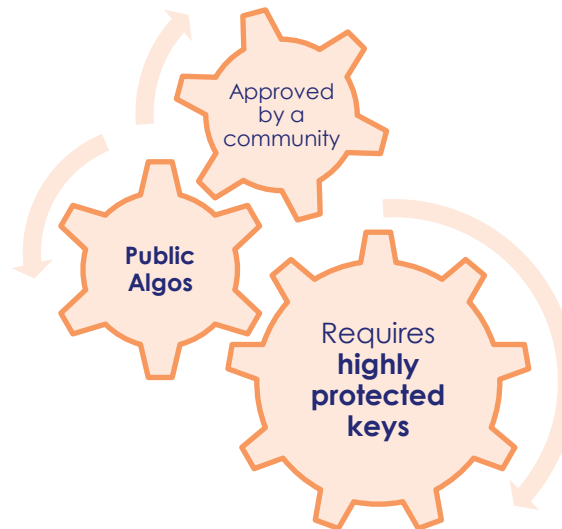
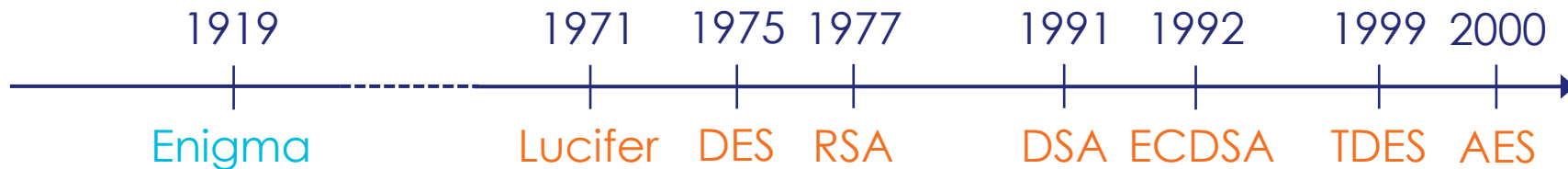






Secret algorithm

Public algorithm / Secret key



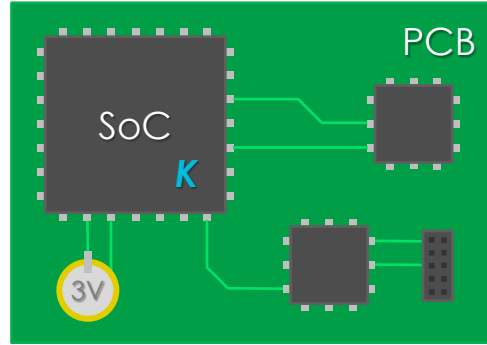
Non-invasive attacks

Passive (observation)

- On-board probing
- Side-channel attacks

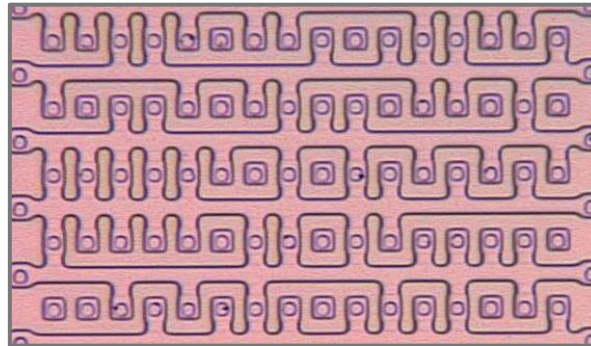
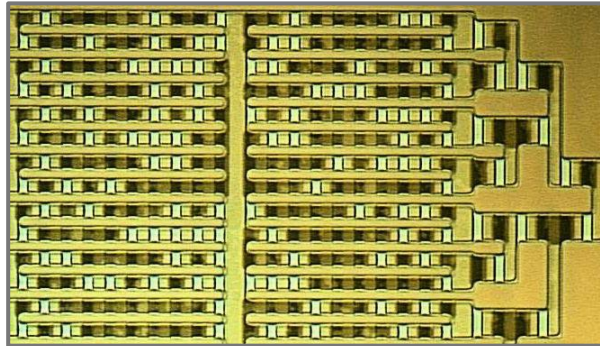
Active (perturbation)

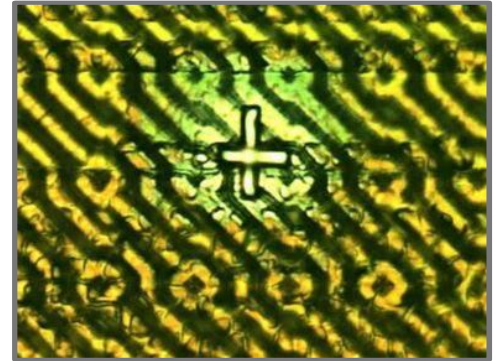
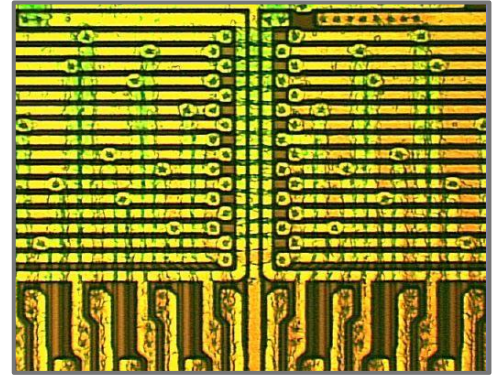
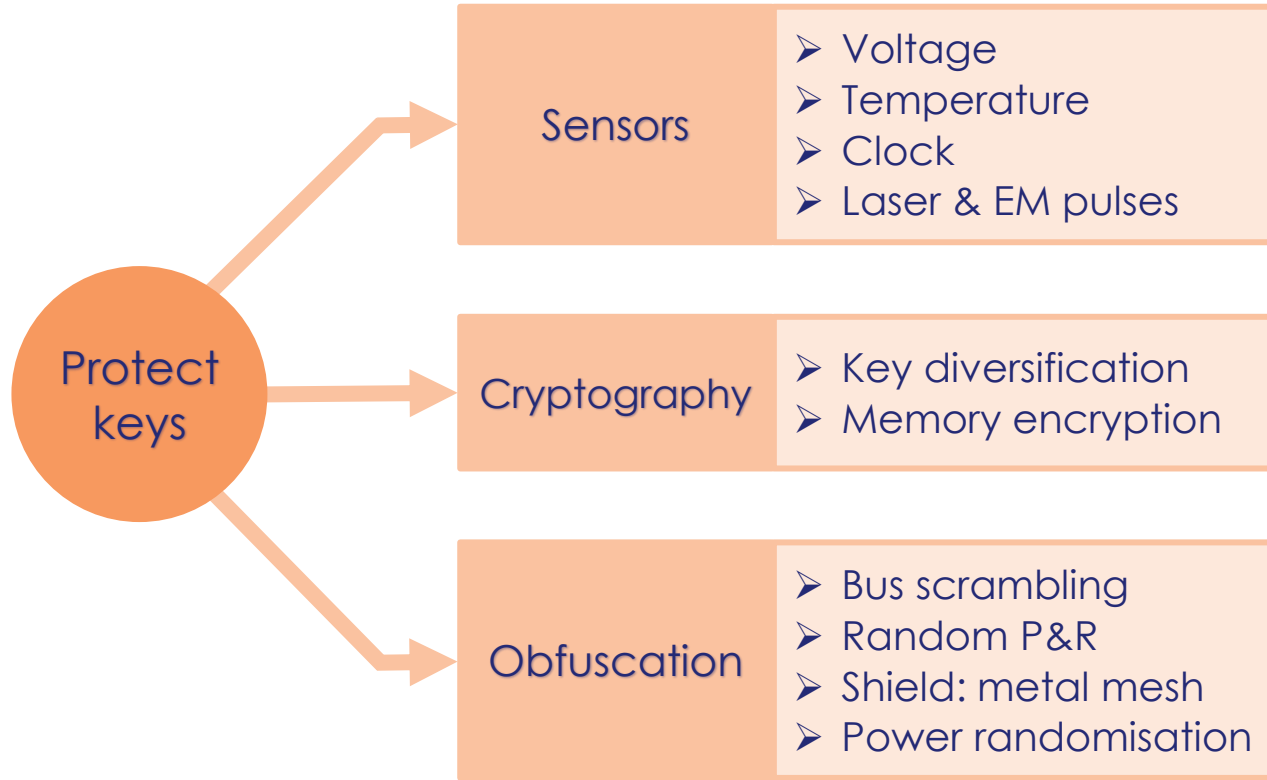
- Over/under V, T° or clock
- Voltage, laser, clock or EM glitches



Invasive attacks

- Chemical & laser etching
- On-chip microprobing
- Layout reconstruction
- Memory content recovery
- Electron Beam Tester (EBT)
- FIB-SEM nanofabrication





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Principle

- Acts as a device fingerprint
- Generates a per-chip unique identifier
- Exploits the random variations of the devices' parameters

Benefits

- Much stronger protection than obfuscation
- Key generation without storage
- Accessible without security knowledge as an IP block
- Ground for full security of an ASIC / SoC



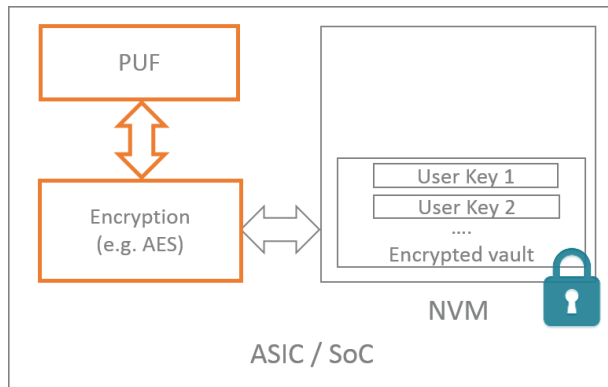
Challenges

- Unclonable: robust against counterfeiting
- Uncontrollable: robust against invasive attacks
- Unpredictable: robust against reverse engineering
- Invariant: stable across voltage, temperature and aging



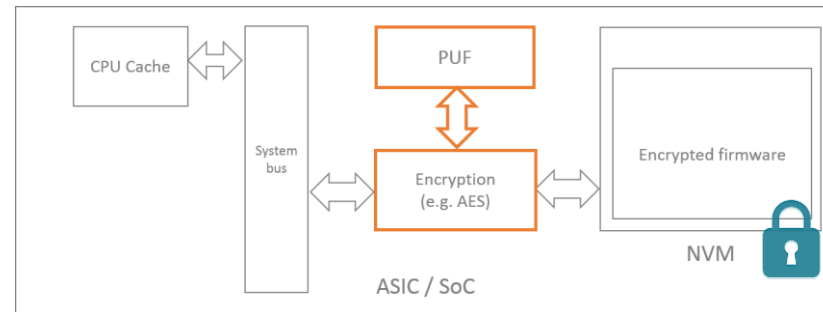


Key Vault



- Keys are the most valuable assets
- Physical key protection available to non security experts
- Stronger than obfuscation

Software IP Protection



- Software IP is gaining value
- PUF with encryption
 - provides the strongest protection
 - enables revenue protection



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Delay based

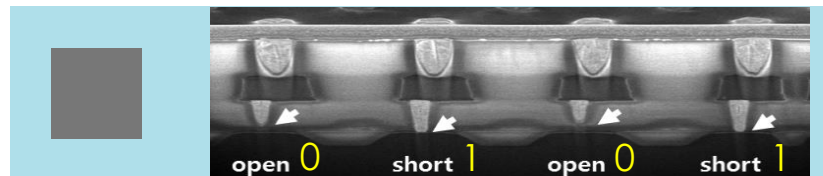
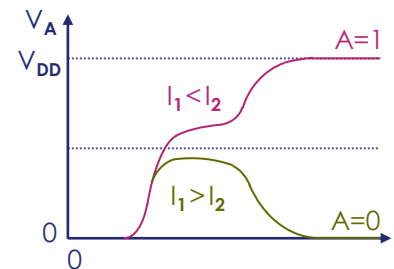
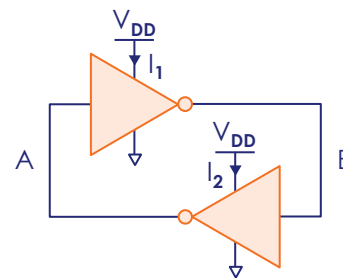
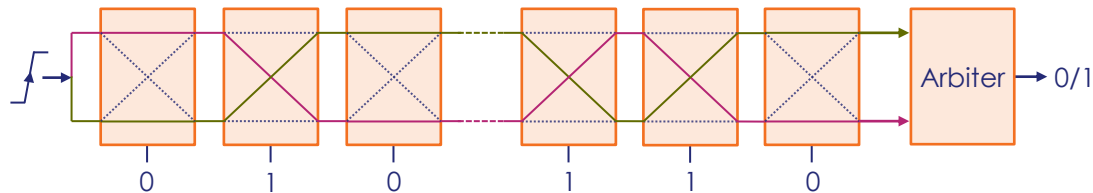
- Arbiter
- Ring oscillator
- Glitch

Memory based

- SRAM
- Latch

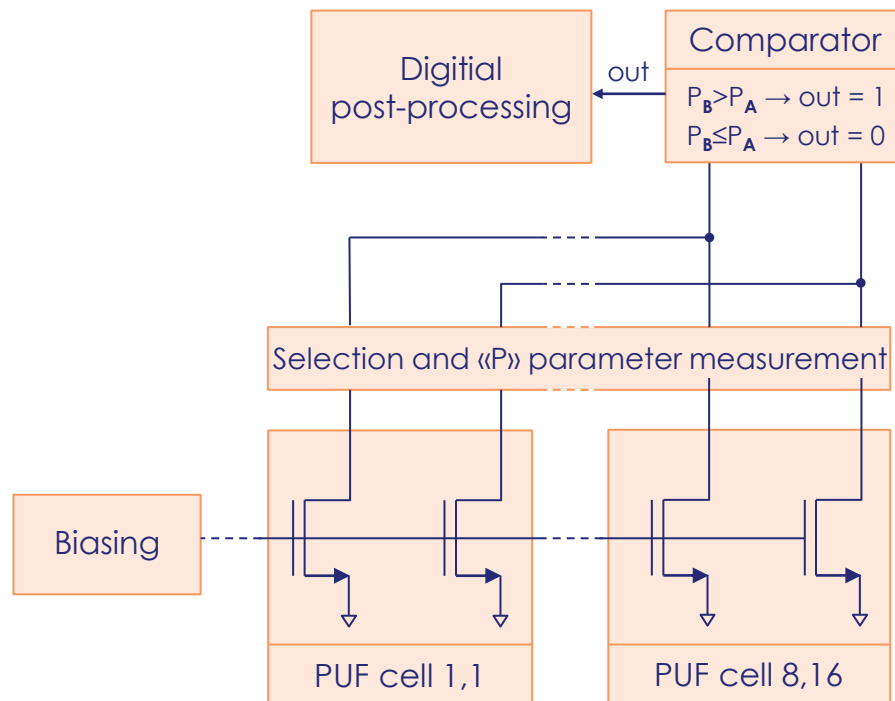
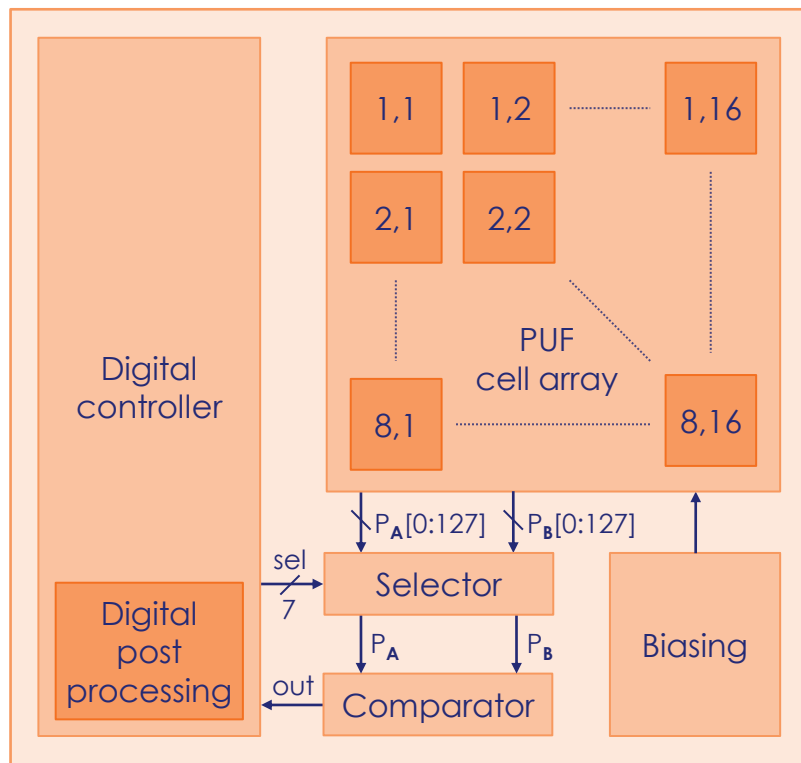
Process based

- V_{GS} or V_{DS}
- Via

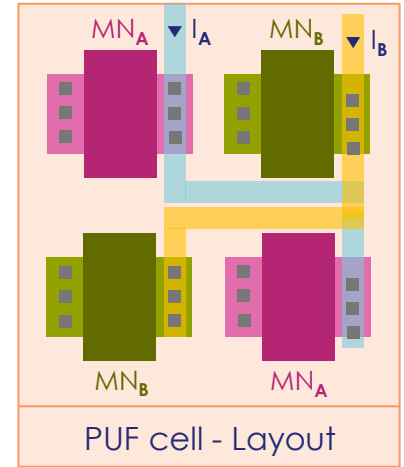
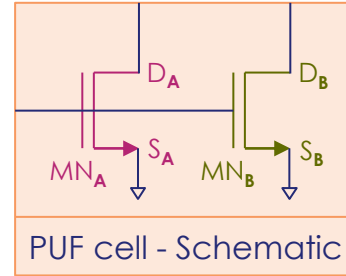
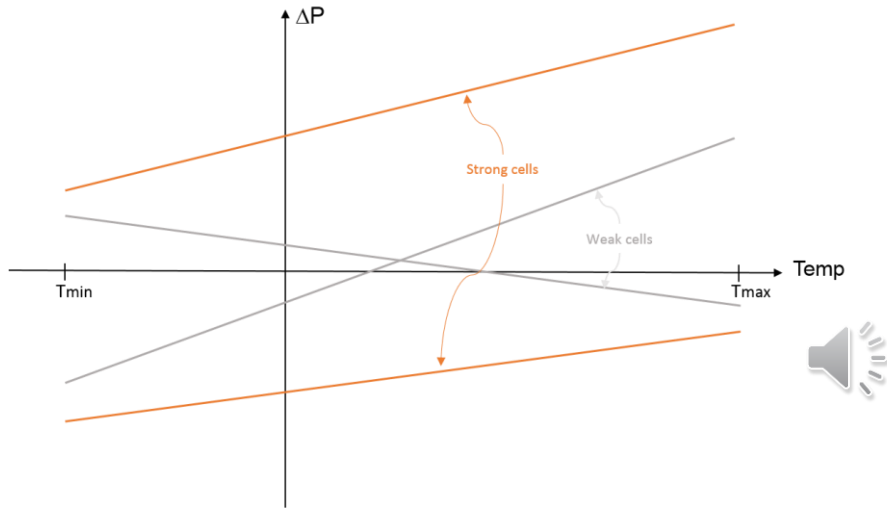


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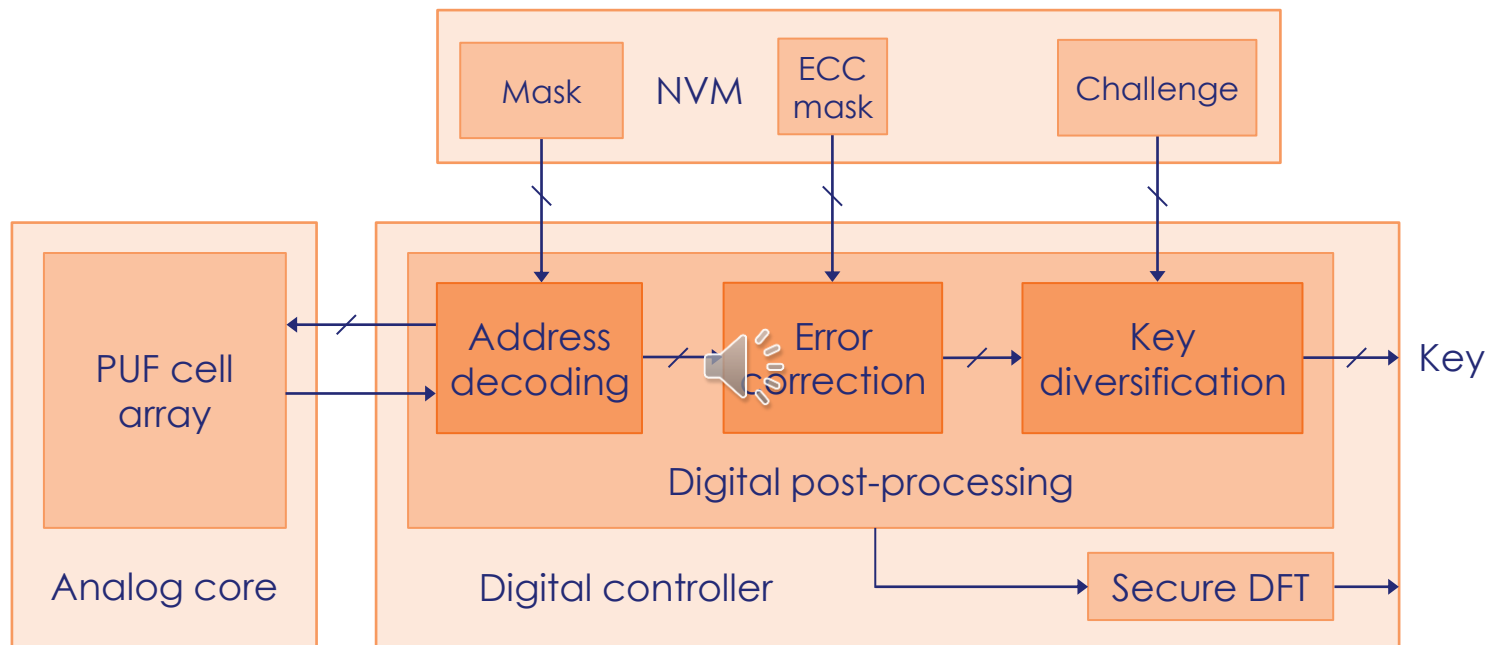


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Weak cells are discarded

- Naturally reliable
- 100 million PUF deployed
 - 1.7 B bits tested
 - 5 ppm before error correction



Enables multiple keys generation to support « one key for one usage »

Performances ($f_{clk}=50$ MHz)

- Active current < 10 μ A
- Stby current < 10 nA
- First key < 210 μ s
- Next keys < 20 μ s

Size

- Digital < 15 k gates
- Analog < 0.02 mm²

Benefits

- **Low-power:** consumption significantly smaller than most alternatives
- **Modelled:** means robust and certifiable
- **Stable and reliable:** sigma optimized by design
- **Secure:** active monitoring of the sub-blocks' integrity
- **Scalable:** the smaller the node, the better the gaussian distribution



INVIA, a Thales company

- Conducts exhaustive security audits
- Assists companies in securing their systems
- Delivers silicon-proven IPs part of EAL5+ ASICs
- Protects more than 2.0 billion deployed devices

Thank you for your attention

